REMARKS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 21-57 are presently active in this case. The present Amendment amends Claims 21, 32, 33, 48 and 55.

In the outstanding Office Action, Claim 32 was objected to because of informalities. Claim 32 was rejected under 35 U.S.C. § 112, second paragraph, as indefinite. Claims 21 and 48 were rejected under 35 U.S.C. § 102(b) as anticipated by Yamaguchi et al. (Japanese patent No. JP 63-047382, herein "Yamaguchi"). Claims 21-23, 25, 27-32, 36-39, 41-43, 45-50, 52 and 54 were rejected under 35 U.S.C. § 102(e) as anticipated by Nagasaki et al. (U.S. Patent No. 5,886,863, herein "Nagasaki"). Claims 24, 40 and 51 were rejected under 35 U.S.C. §103(a) as unpatentable over Nagasaki, in view of Zehnpfennig et al. (U.S. Patent No. 4,385,434, herein "Zehnpfennig"). Claims 26, 44 and 53 were rejected under 35 U.S.C. §103(a) as unpatentable over Nagasaki. Claims 33-35 and 55-57 were rejected under 35 U.S.C. §102(e) as anticipated by Nagasaki.

First, Applicants wish to thank Examiner Patel for the courtesy of an interview granted to Applicants' representative on June 17, 2004, at which time the outstanding issues in this case were discussed. Arguments and claim amendments similar to those discussed with the Examiner are included in this Amendment. The Examiner indicated he would further consider such amendments and arguments when formally presented in a filed response.

To clarify the claims, independent Claims 21, 33, 48 and 55 are amended to recite "a conductor layer directly contacting a surface of a semiconductor wafer during a probing of a semiconductor wafer." The amendment of these claims find support in the specification as

originally filed.[1] Therefore, amended Claims 21, 33, 48 and 55 are not believed to raise a question of new matter.[2] In light of the amendments made to the independent Claims, the rejections are now moot.

In response to the rejection of Claim 32 under 35 U.S.C. § 112, second paragraph, Claim 32 is amended to correct the noted informalities and indefiniteness, to recite "The wafer prober according to Claim 21, which performs the probing of the semiconductor wafer by pressing a probe card on the wafer and applying an electric voltage to the semiconductor wafer." The amendment finds support in the disclosure as originally filed.[3] Therefore, Claim 32 is not believed to raise a question of new matter.[4]

In response to the rejection of Claims 21 and 48 under 35 U.S.C. § 102(b), Applicants respectfully request reconsideration of these rejections and traverse the rejections as discussed next.

Claims 21 and 48 relate to a wafer prober or a ceramic substrate with a conductor layer directly contacting a surface of the semiconductor wafer during a probing of the semiconductor wafer.

However, Yamaguchi discloses a **wiring board** comprising a nitride ceramic board and a metal layer on the surface thereof.[5] However, the wiring board is not used as a **wafer prober** and the electric conductor will not directly contact a surface of the semiconductor wafer during a probing of the semiconductor wafer. Yamaguchi does not teach anything about a wafer prober, and does not suggest to use the wiring board for probing a wafer. In other words, Yamaguchi does not teach or suggest a wafer prober for probing semiconductor

[1] See for example in Applicants' specification at page 1, lines 26-30 and Fig. 12
[2] See MPEP 2163.06 stating that "information contained in any one of the specification, claims or drawings of the application as filed may be added to any other part of the application without introducing new matter."
[3] For example on page 1, lines 17-20 and 26-30.
[4] See MPEP 2163.06 stating that "information contained in any one of the specification, claims or drawings of the application as filed may be added to any other part of the application without introducing new matter."
[5] See Yamaguchi in the abstract

wafers having a ceramic substrate and a conductor layer directly contacting a surface of the semiconductor wafer during a probing of the semiconductor wafer.

Additionally, Applicants made a typing error in the last Amendment submitted on September 15, 2003 on page 17, line 3-4, reciting "Yamaguchi et al does contain a disclosure related to a wafer prober". In fact, Yamaguchi does **not** teach or suggest a wafer prober or disclose anything related to a wafer prober. Applicants intended to state that "Yamaguchi et al does **not** contain a disclosure related to a wafer prober."

Therefore, Yamaguchi fails to teach or suggest every feature recited in Claims 21 and 48, so that Claims 21 and 48, and the Claims dependent thereof, are believed to be patentably distinct over Yamaguchi. Accordingly, Applicants respectfully traverse, and request reconsideration of the rejections based on Yamaguchi.[6]

In response to the rejection of Claims 21-23, 25, 27-32, 36-39, 41-43, 45-50, 52 and 54 under 35 U.S.C. § 102(b), as well as the rejection of Claims 33-35 and 55-57 under 35 U.S.C. § 102(b) over Nagasaki, Applicants respectfully request reconsideration of these rejections and traverse the rejections as discussed next.

Independent Claims 21, 33, 48 and 55 relate to a wafer prober or a ceramic substrate for probing a semiconductor wafer with a conductor layer formed on a surface of the ceramic substrate, and the conductor layer directly contacts a surface of the semiconductor wafer during a probing of the semiconductor wafer.

As explained in Applicants' specification, the claimed invention improves conventional wafer probers because it is lightweight, excellent in thermal response kinetics

[6] See MPEP 2131: "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," (Citations omitted) (emphasis added). See also MPEP 2143.03: "All words in a claim must be considered in judging the patentability of that claim against the prior art."

and reduced warpage upon pressing with a probe card. The claimed invention thus leads to improved wafer prober.[7]

Nagasaki, however, discloses a **wafer support member**, used as a plasma generating electrode.[8] Nagasaki furthermore recites that the wafer support member is used in a semiconductor manufacturing apparatus in the process of fixing the semiconductor wafer which is the object of attraction for PVD (physical vapor deposition), CVD (Chemical vapor deposition), etching or other processing.[9] However, Nagasaki does not teach or suggest anything in the fields of **wafer probes** for probing of the semiconductor wafer, and is also not concerned with checking characteristics of wafers.[10]

Furthermore, Nagasaki discloses a holding surface formed on each electrode with an aluminum nitride film[11] and silicon wafers attracted to the attraction surface 203a on the aluminum nitride film 203.[12] However, Nagasaki fails to teach a conductor layer formed on a surface of said ceramic substrate and that the conductor layer is directly contacting a semiconductor wafer during a probing of the semiconductor wafer. On the contrary, Nagasaki explicitly teaches a nitride film on the surface of the base body as an insulating layer[13] and aluminum nitride films 103 of various film thicknesses were prepared as insulating films.[14] An insulating layer made of aluminum nitride is **not** a conductor layer formed on a surface of a ceramic substrate.

Therefore, Nagasaki fails to teach or suggest every feature recited in the claims, so that Claims 21-23, 25, 27-39, 41-43, 45-50, 52 and 54-57 are believed to be patentably

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[7] See Applicants' specification at page 2, lines 15-20
[8] See Nagasaki at col. 1, ll. 4-7 and in the Abstract
[9] See Nagasaki at col. 1, ll. 8-13
[10] See Applicants' specification at page 1, lines 17-20
[11] See Nagasaki at col. 32, ll. 57-64
[12] See Nagasaki at col. 17, ll. 27-29
[13] See Nagasaki at col. 2, ll. 38-41
[14] See Nagasaki at col. 14, ll. 24-26 and Fig. 5

distinct over Nagasaki. Accordingly, Applicants respectfully traverse, and request reconsideration of, the rejections based on Nagasaki.

In response to the rejection of Claims 24, 40 and 51 under 35 U.S.C. § 103(a), as unpatentable over Nagasaki in view of Zehnpfennig, Applicants respectfully request reconsideration of these rejections and traverse the rejections as discussed next.

As mentioned above, the applied prior art Nagasaki discloses a wafer support member used as plasma generating electrode. Nagasaki, however, fails to teach or suggest the claimed conductor layer formed on a surface of a ceramic substrate and that the conductor layer is directly contacting a surface of the semiconductor wafer during a probing of the semiconductor wafer. Applicants respectfully submit, however, that Zehnpfennig also fails to disclose the above mentioned feature related to a conductor layer formed on a surface of the ceramic substrate. Thus, the claims also distinguish over Nagasaki in view of Zehnpfennig.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal Allowance. A Notice of Allowance for Claims 21-57 is earnestly solicited.

Should the Examiner deem that any further action is necessary to place this application in even better form for allowance, the Examiner is encouraged to contact Applicant's undersigned representative at the below listed telephone number.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
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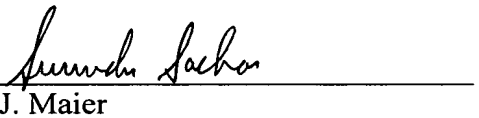

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